

FIG 1

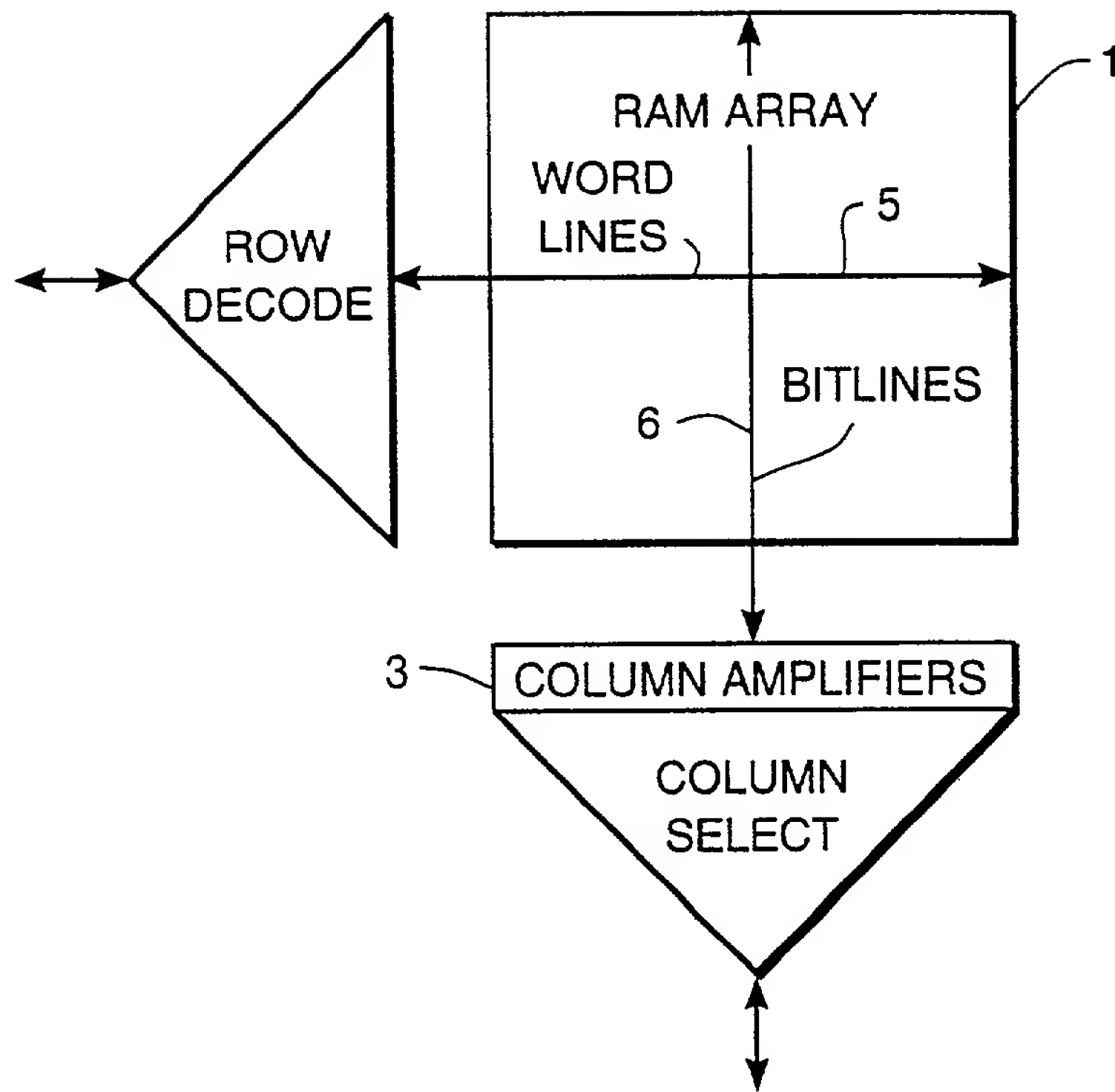


FIG. 2 is a block diagram of a system 100 according to one embodiment of the present invention. The system 100 includes a CPU 11, a ROM 12, a DRAM 13, and a DRAM 14. Each of the CPU 11, ROM 12, and DRAM 13 is connected to a common bus 161. The CPU 11 is connected to the bus 161 via a CPU device interface 11. The ROM 12 is connected to the bus 161 via a ROM device interface 12. The DRAM 13 is connected to the bus 161 via a DRAM device interface 13. The DRAM 14 is connected to the bus 161 via a DRAM device interface 14. The bus 161 is connected to a RESETOUT signal, a RESETIN signal, a BUSDATA[7] signal, a BUSDATA[1] signal, a BUSDATA[0] signal, an ADDRVALID signal, a CLOCK1 signal, a CLOCK2 signal, a VREF signal, a GND signal, and a VDD signal.

FIG. 2

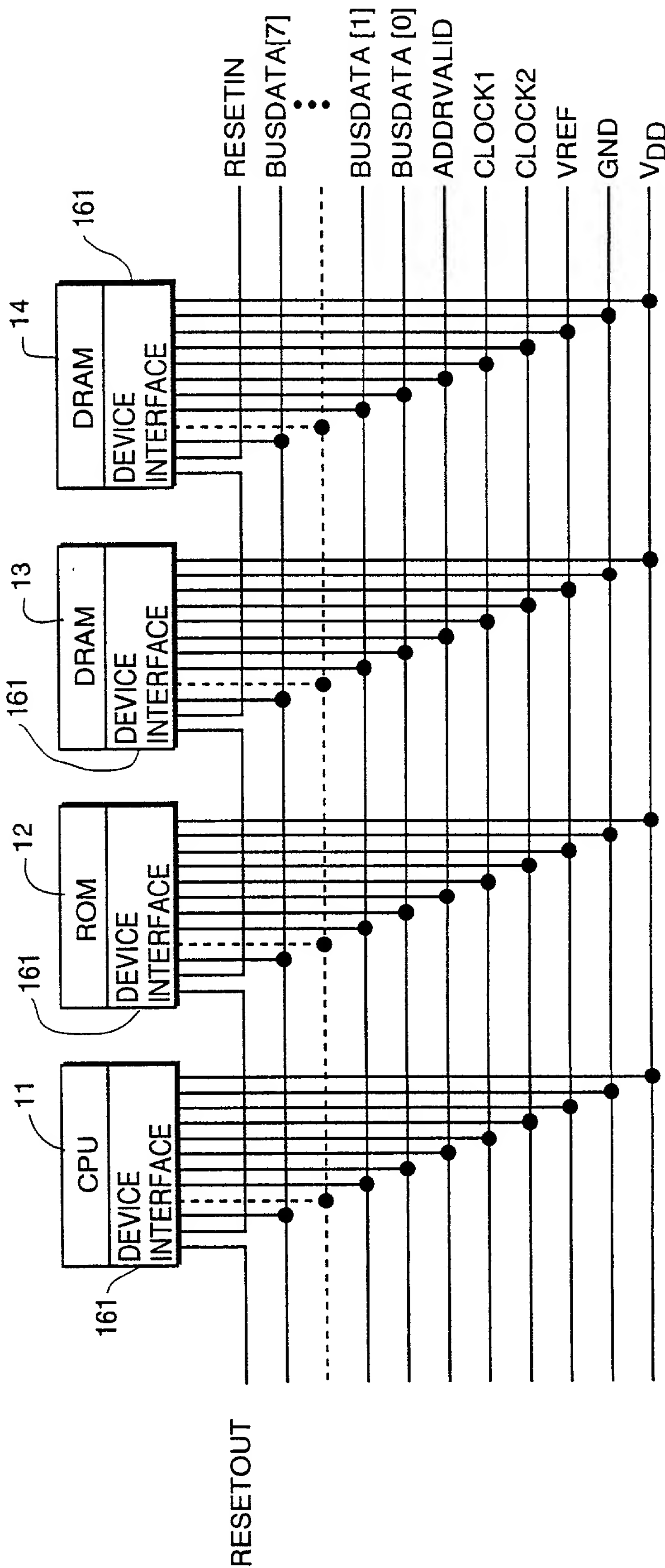
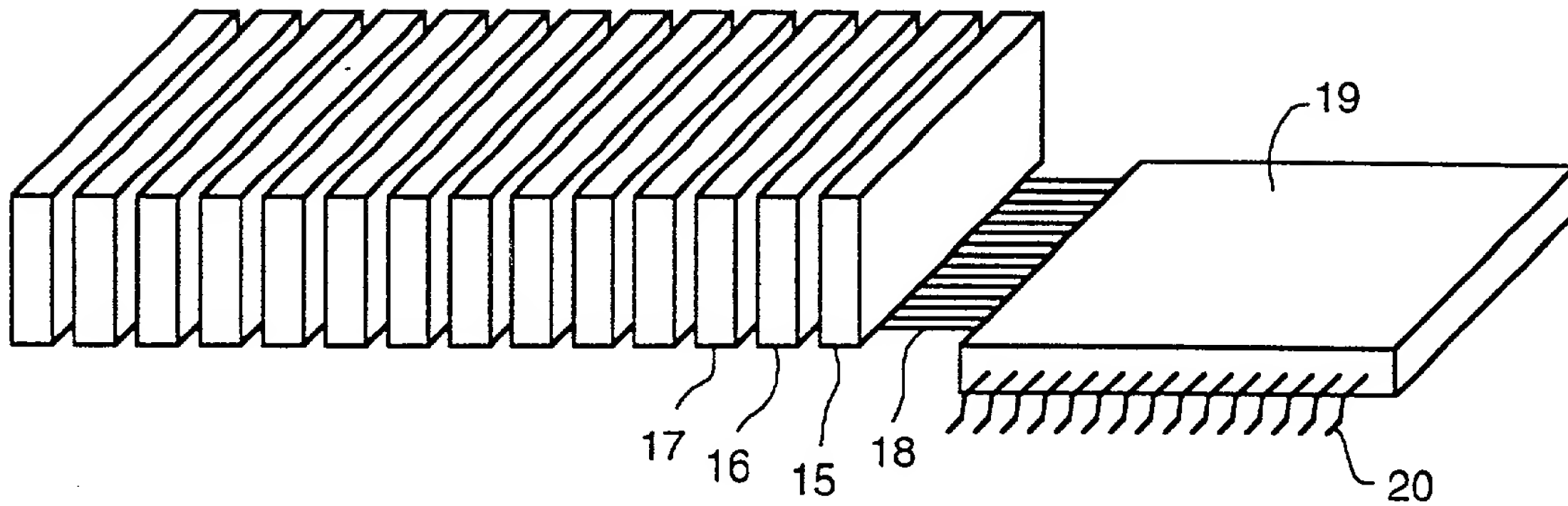


FIG 3



REGULAR ACCESS

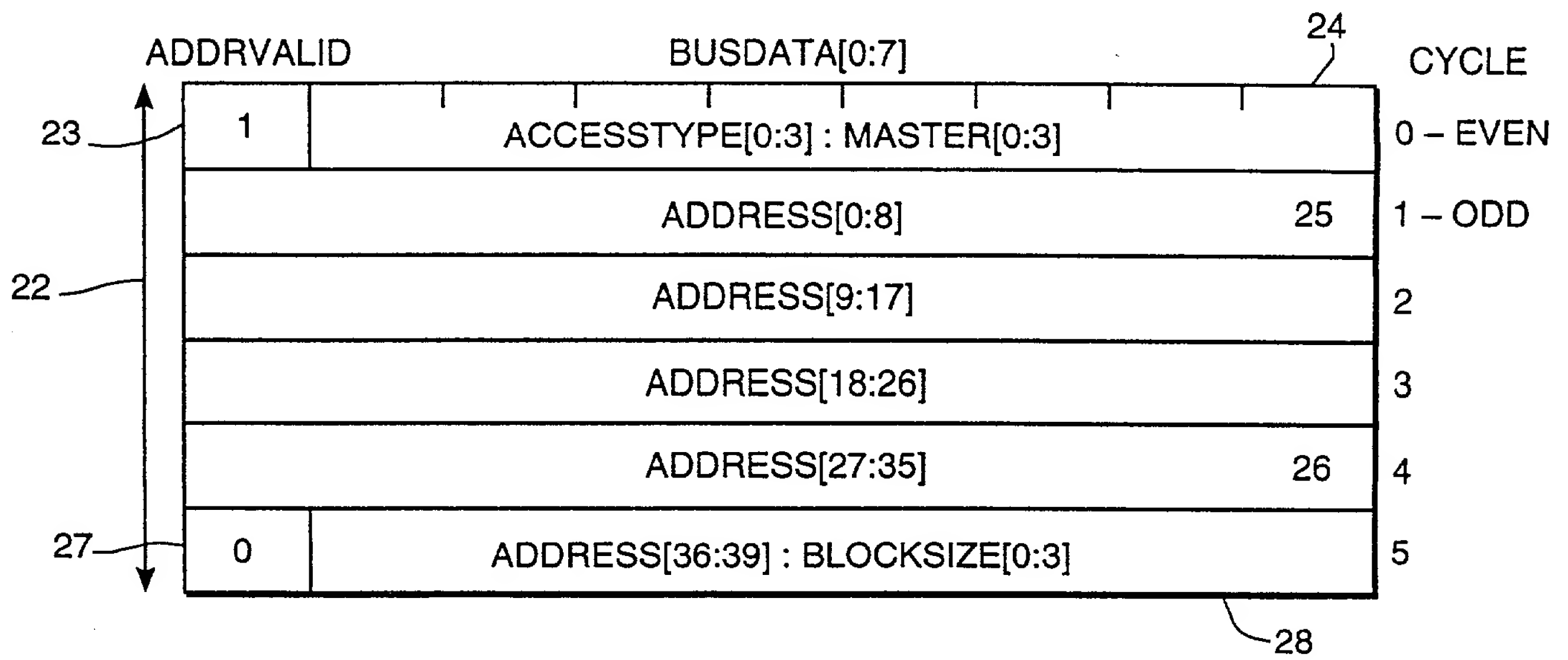


FIG 4

REJECT (NACK) CONTROL PACKET

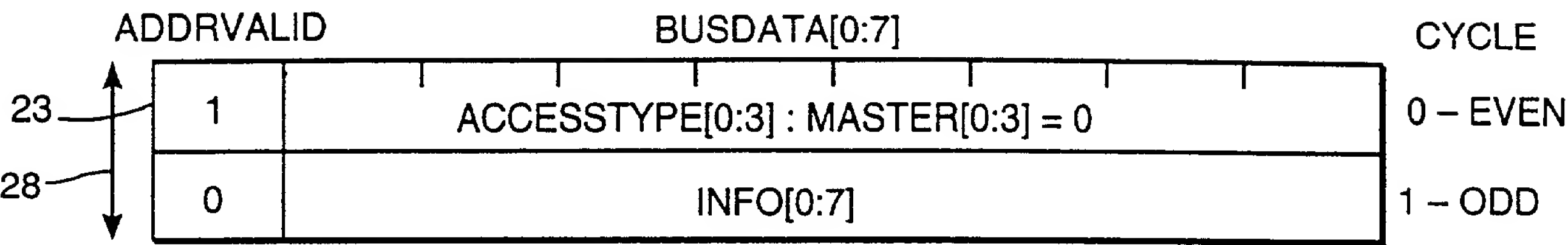


FIG 5

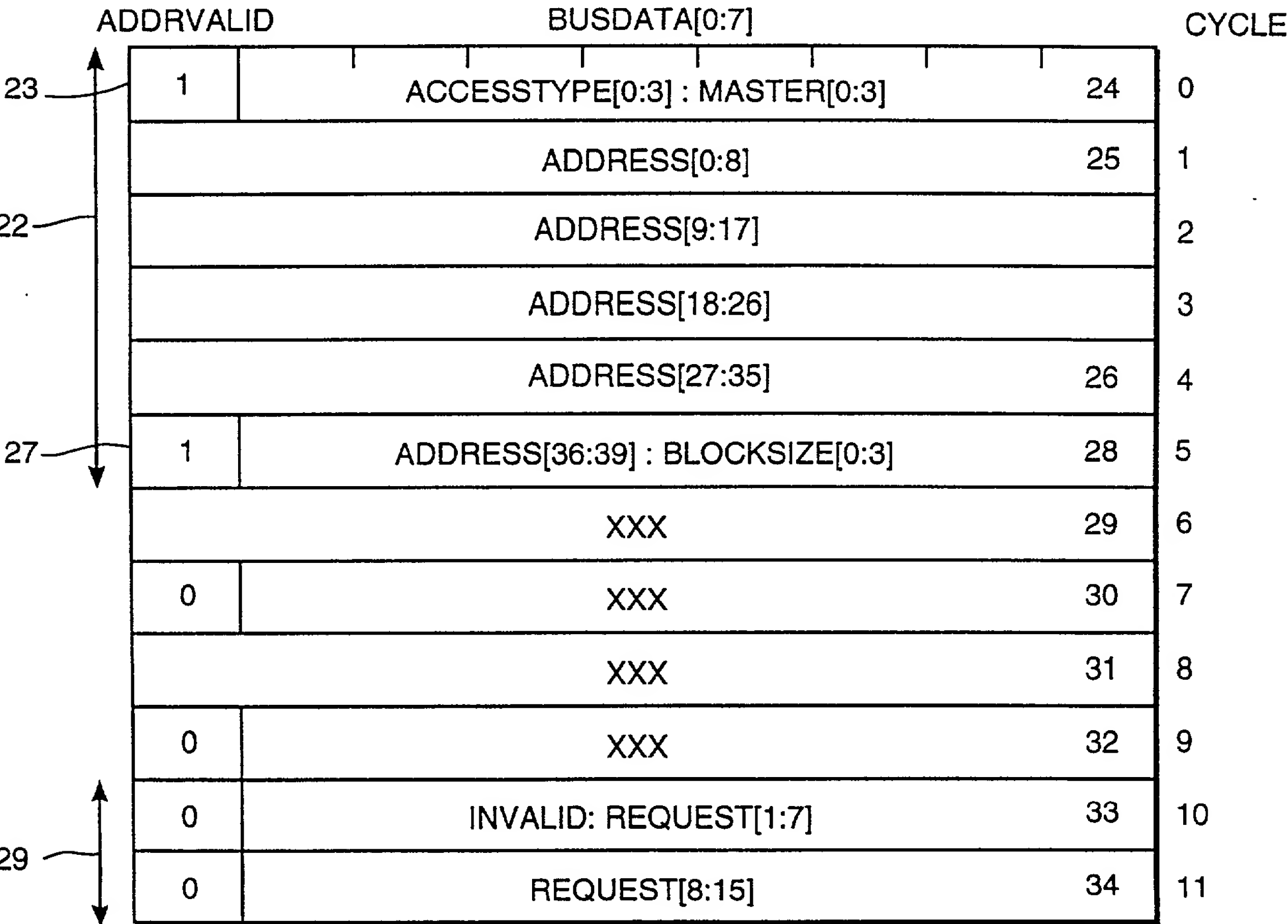


FIG 6

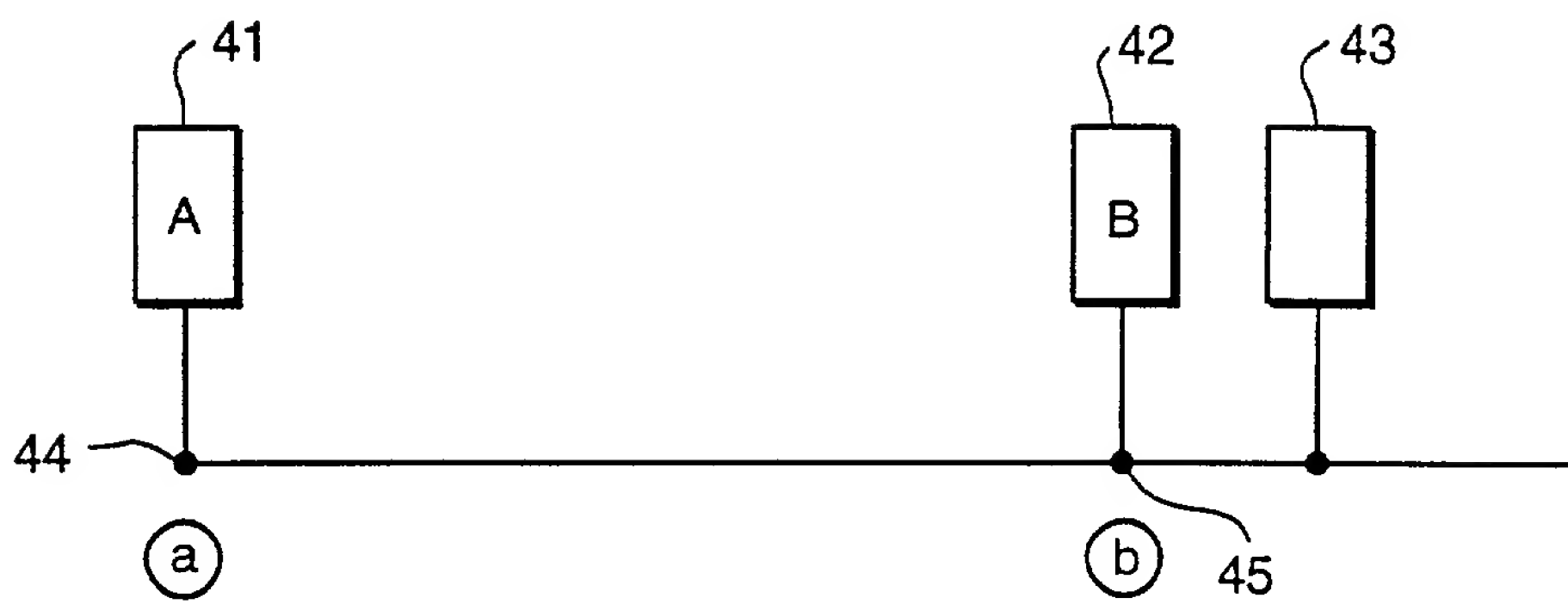


FIG 7A

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VOLTAGE LOGICAL
VALUE

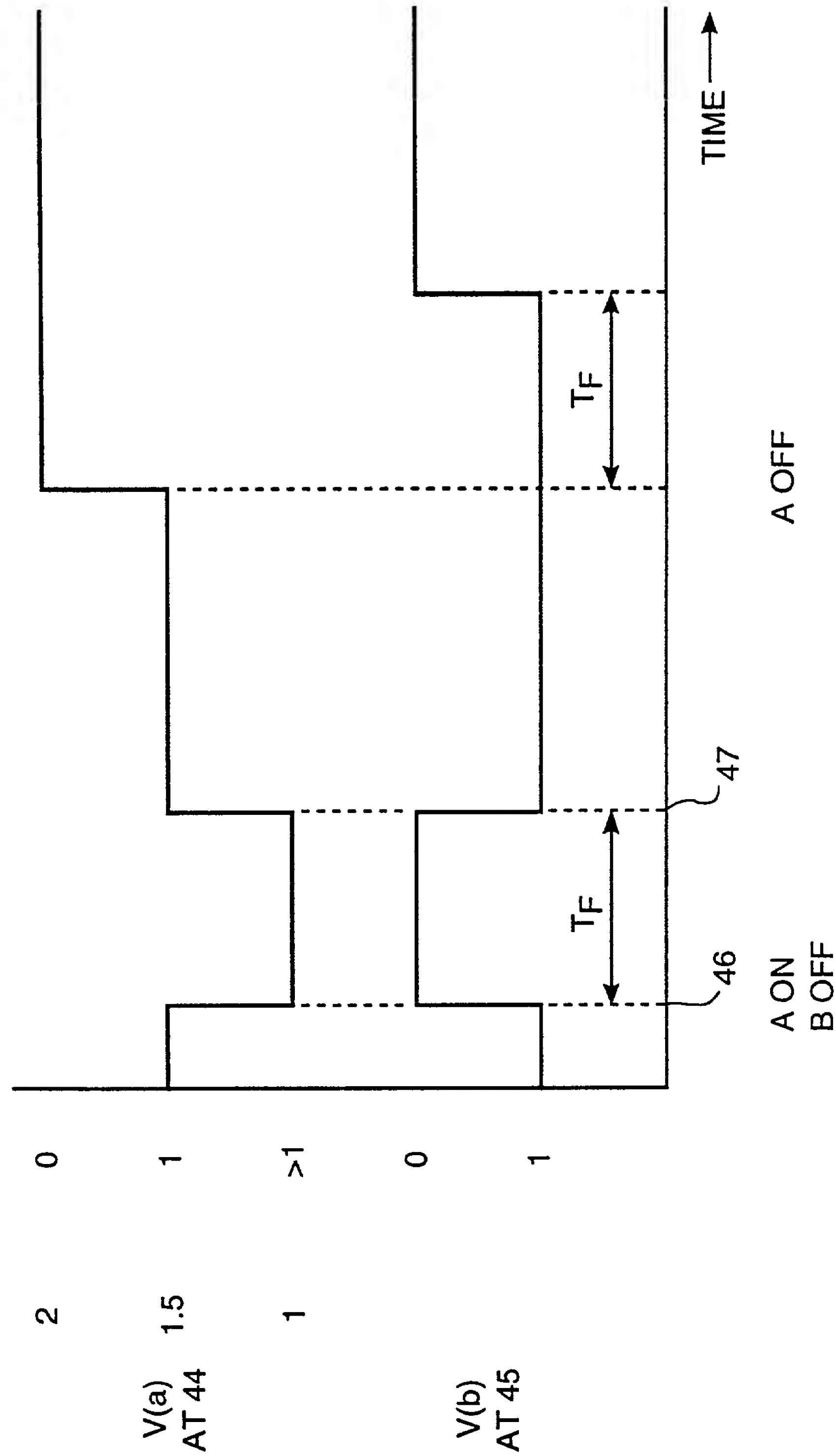


FIG 7A

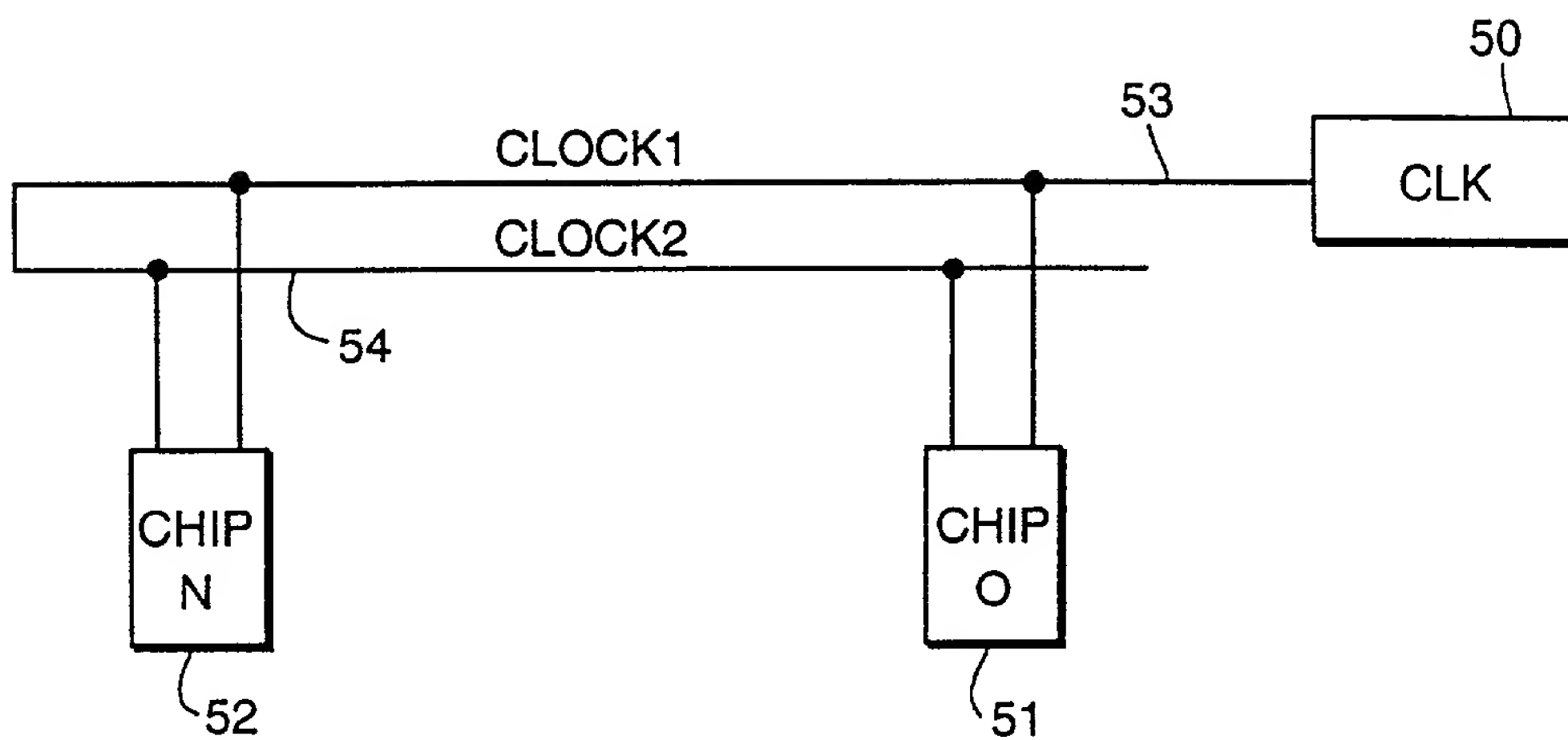


FIG 8A

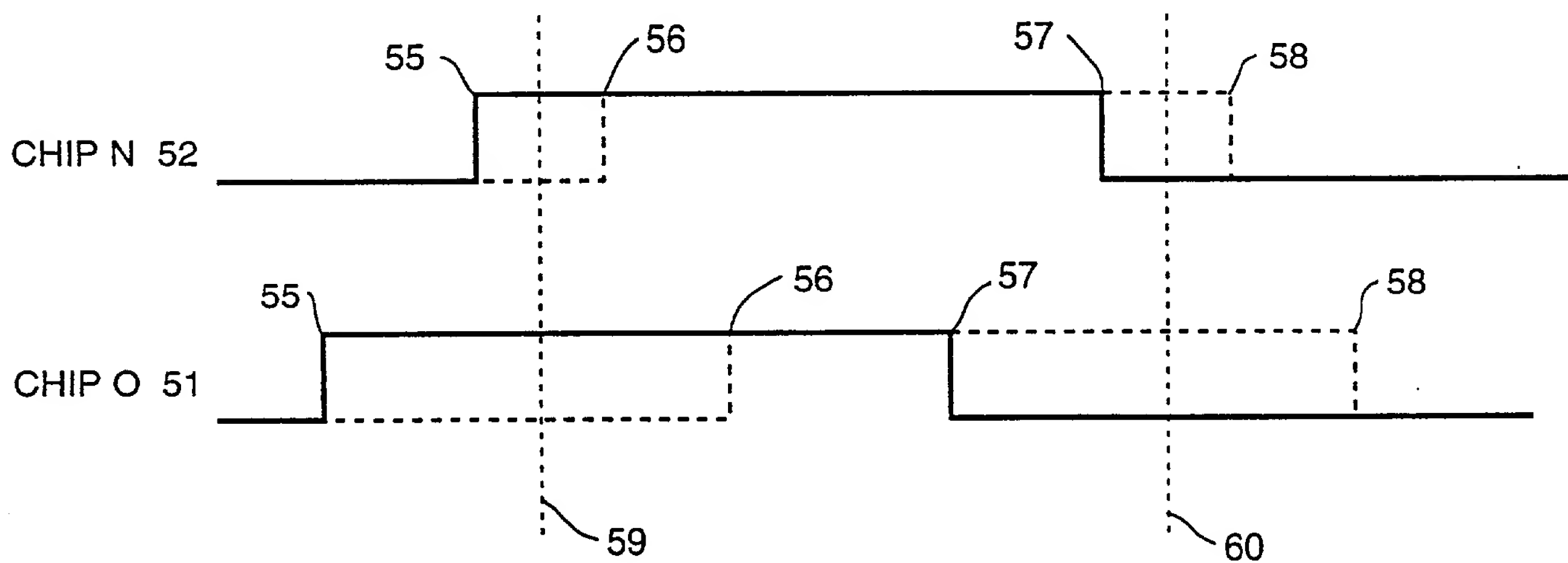
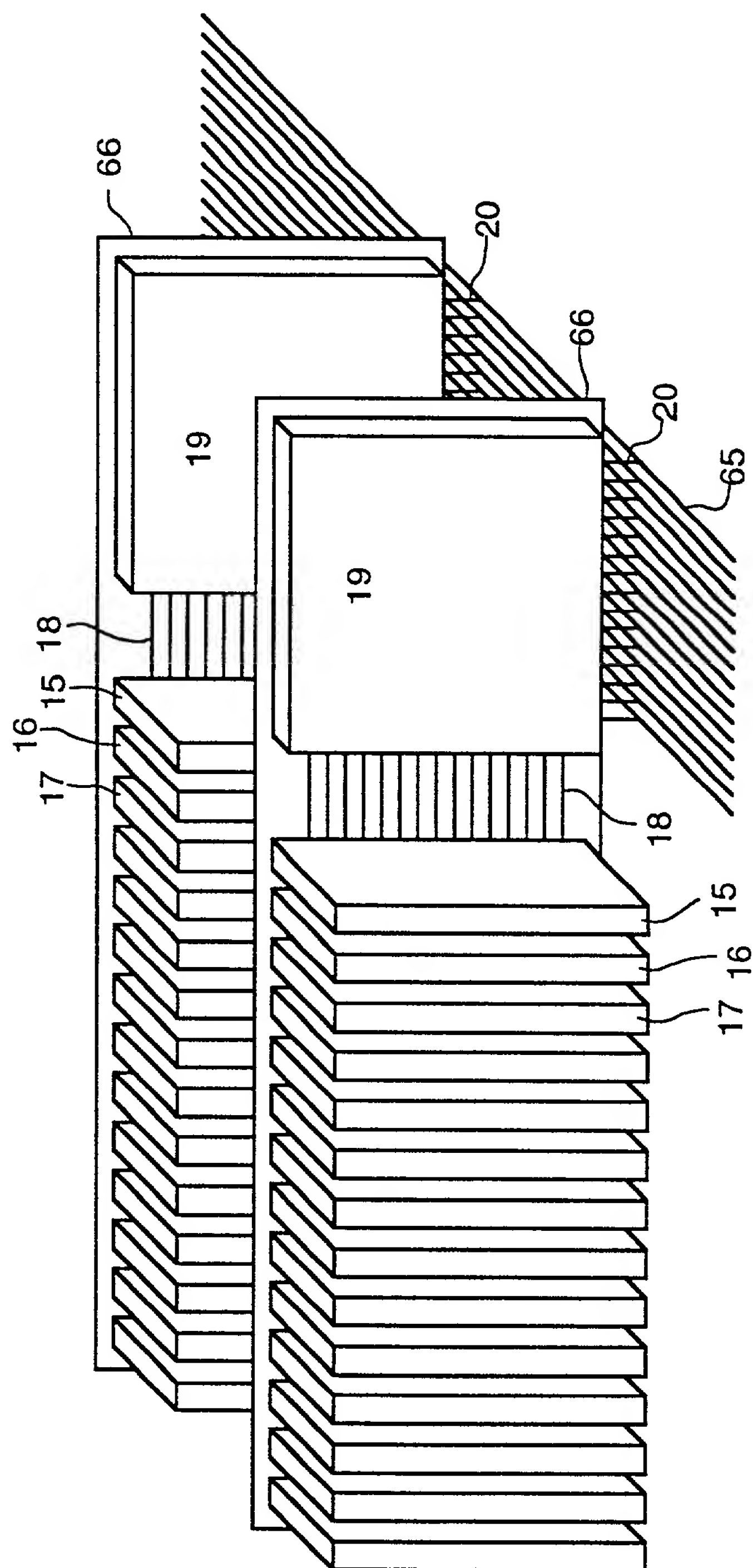


FIG 8B

THE



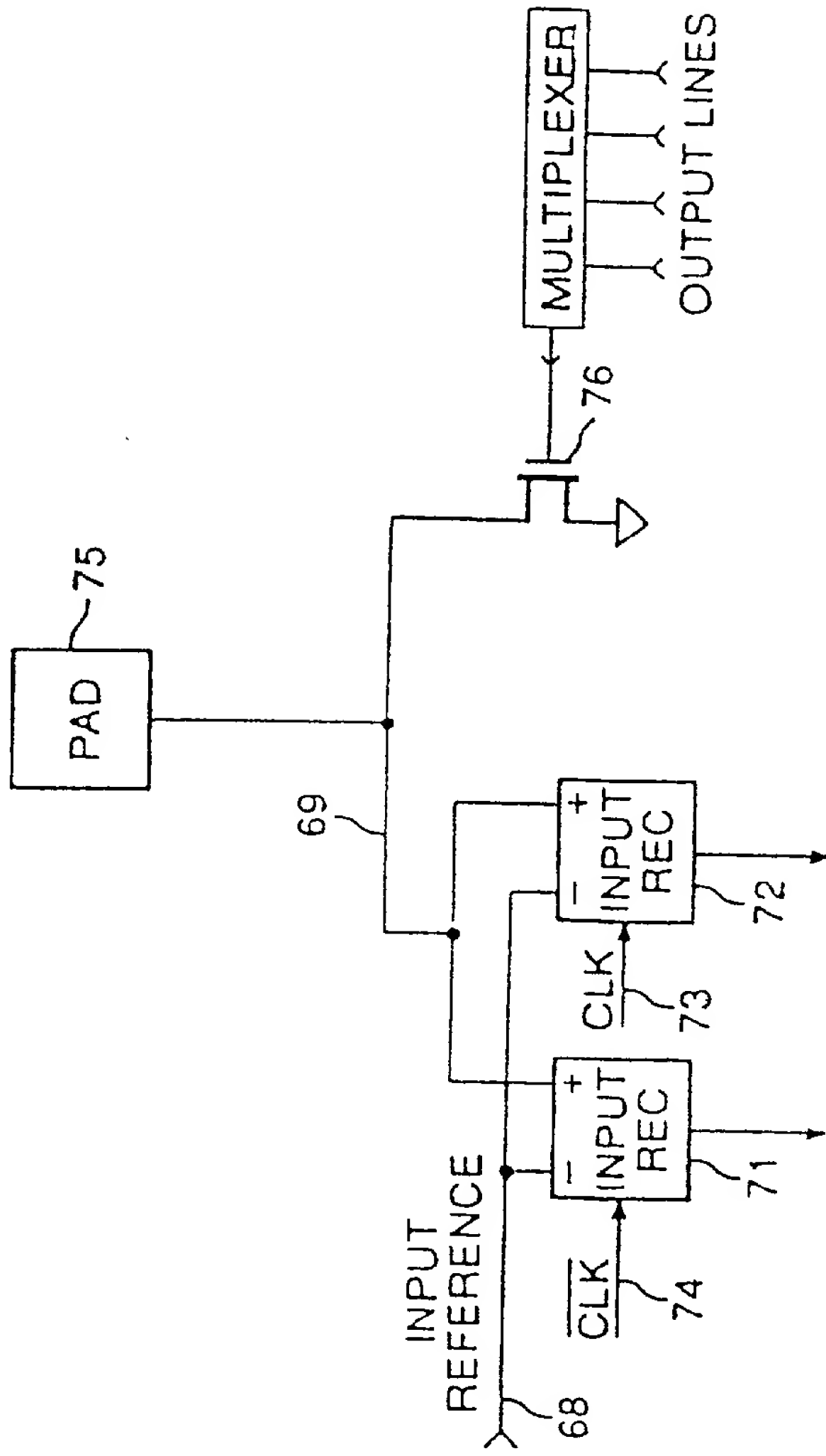


FIG. 10

FIG 11

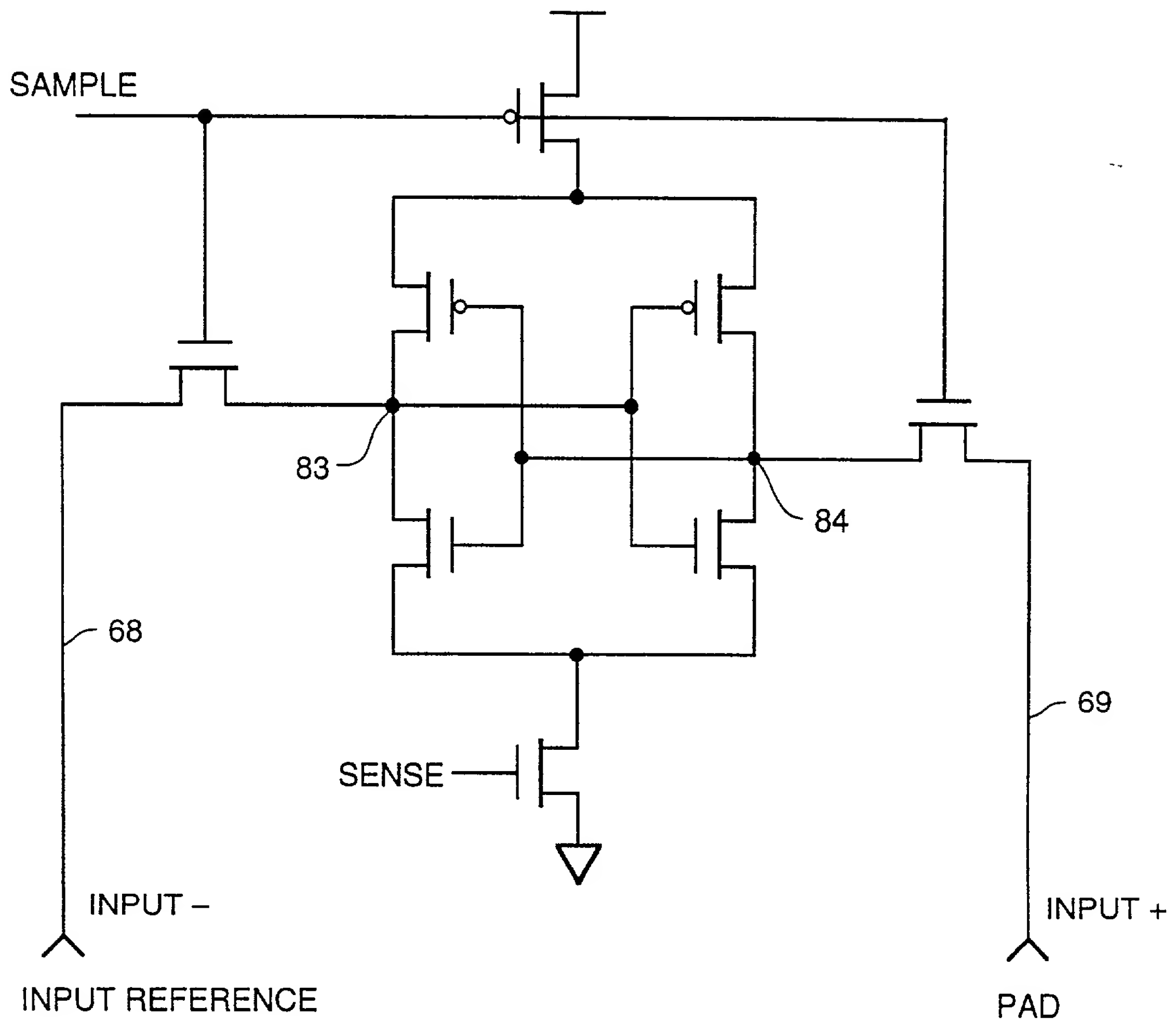
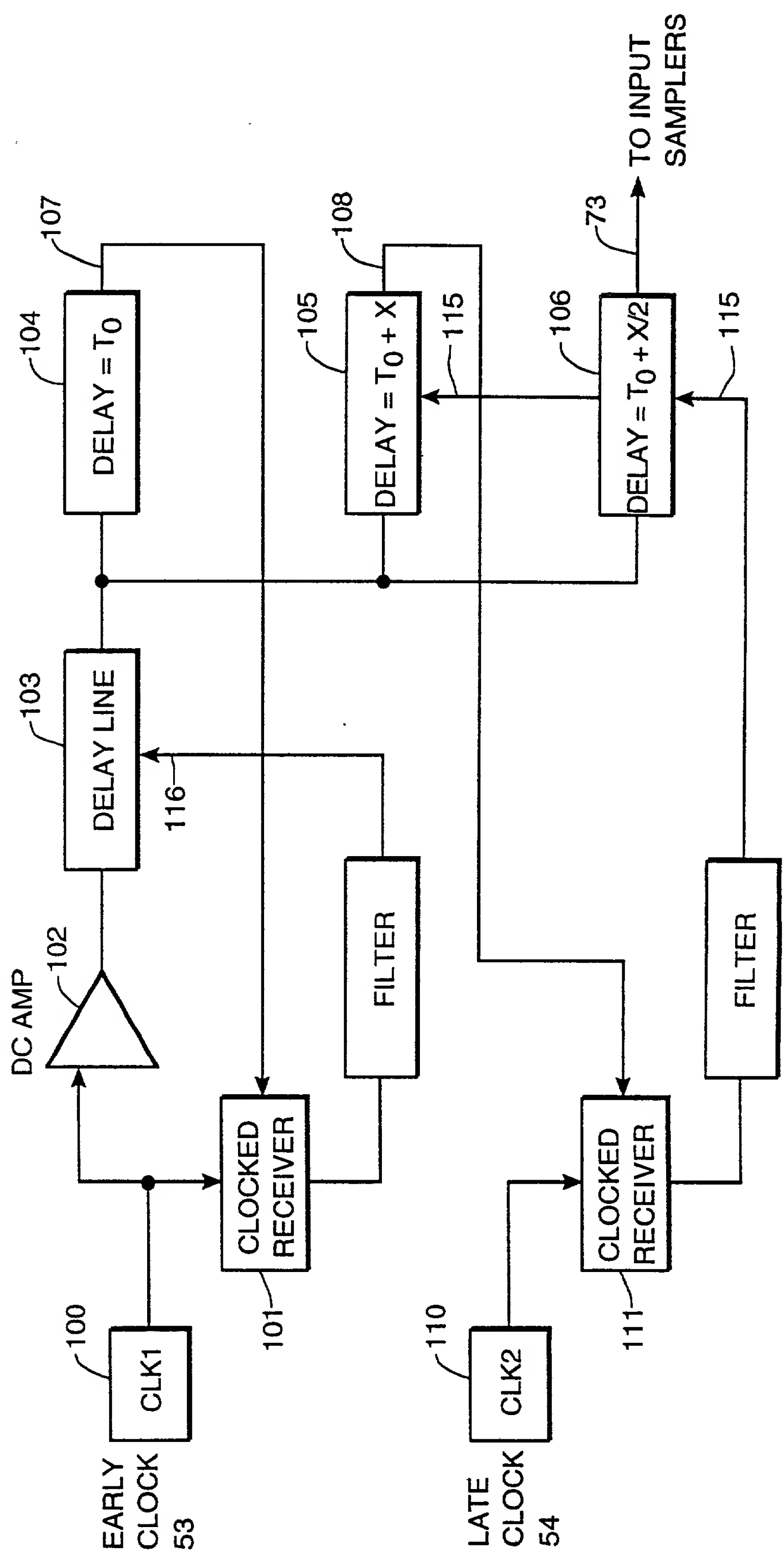
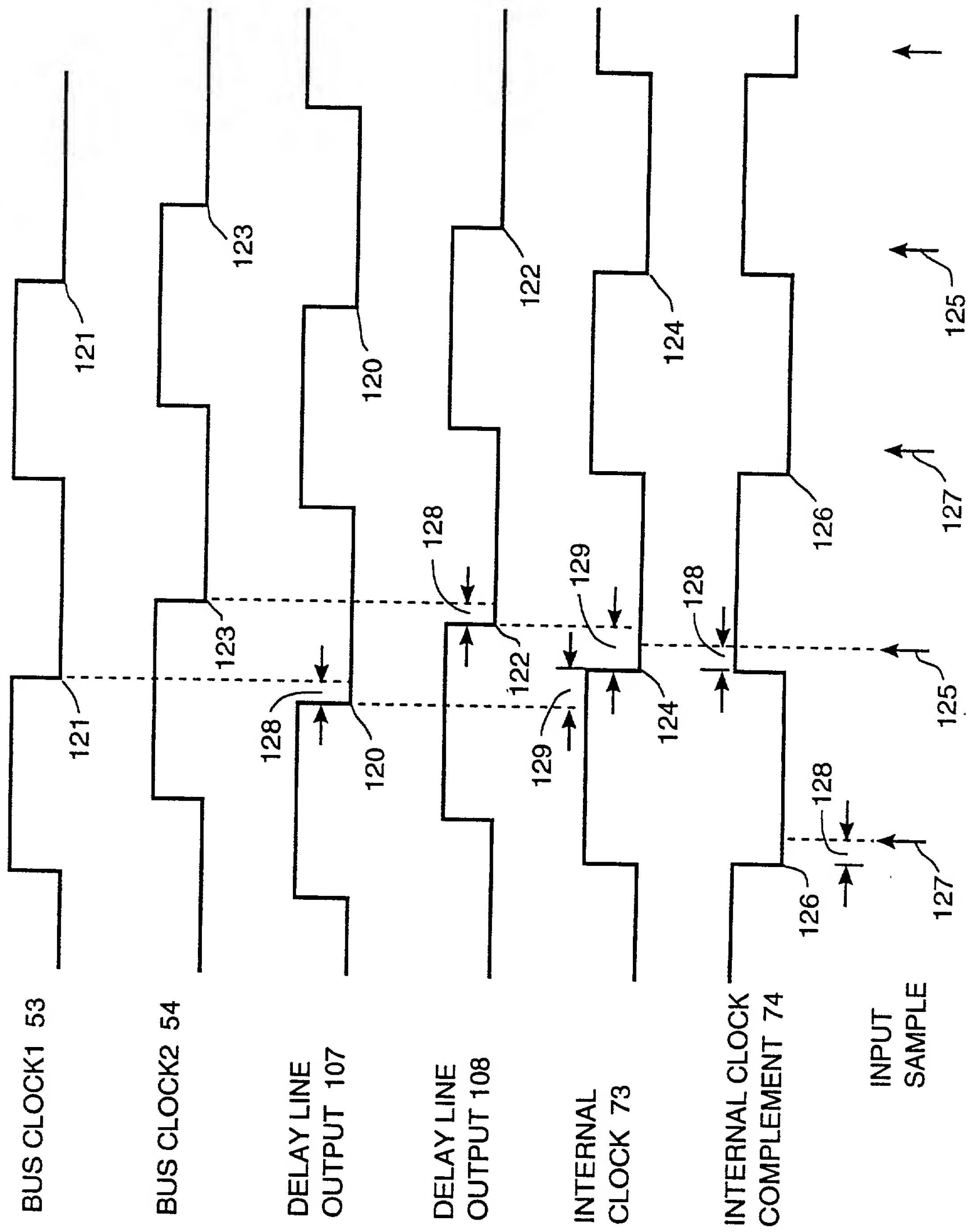


FIG 12





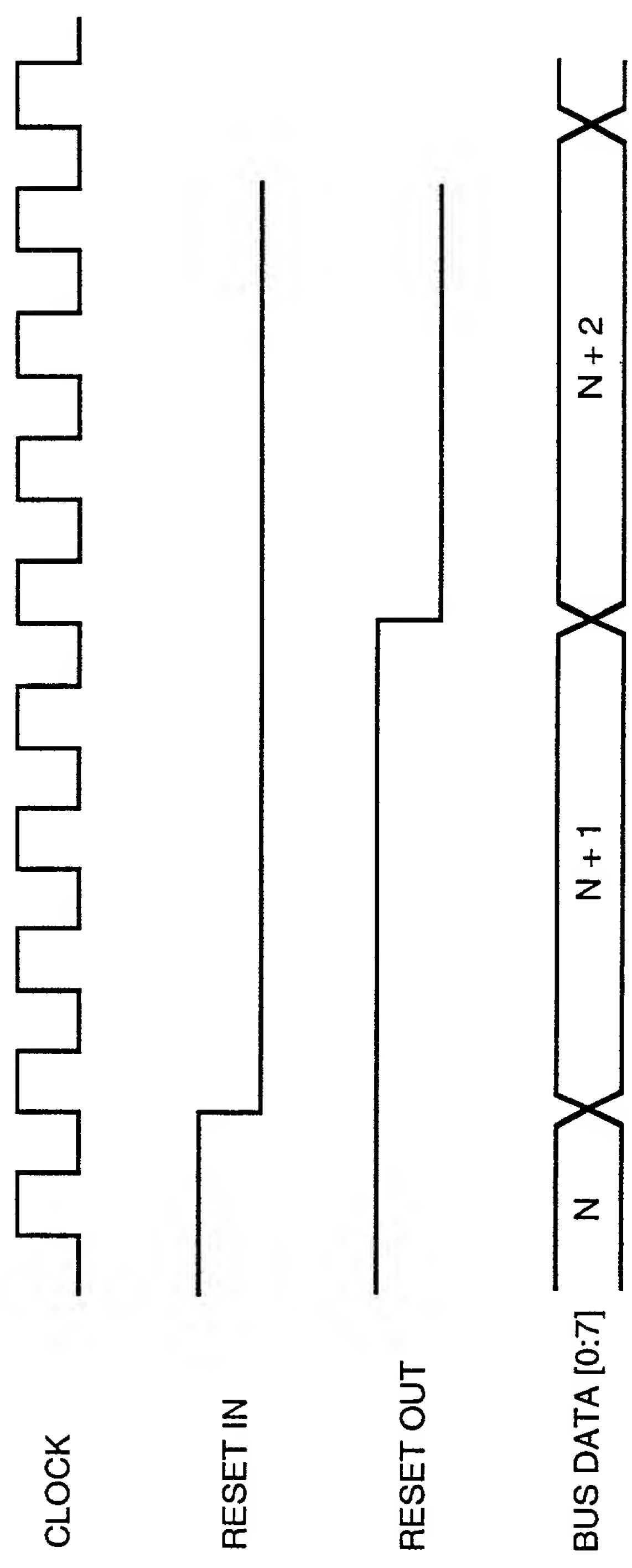


FIGURE 14-14

FIG 15

